NEX92X30-Q100

300 mA, dual-channel antenna LDO with current sensing

Rev. 1 — 1 August 2025 **Product data sheet**

1. General description

The NEX92x30-Q100 devices are dual-channel, high-voltage low-dropout (LDO) regulators with current sensing, they are designed to operate with a wide range of voltage from 4 V to 40 V (45 V load dump protection). These devices provide power supply for low noise amplifiers with an active antenna through a coax cable with 300 mA per channel. It provides an adjustable output voltage from 1.5 V to 20 V for each channel.

These devices provide diagnostics through current sensing and error pins. To monitor the load current, a high-side current-sense circuitry provides a proportional analog output to the sensed load current. Accurate current sensing allows detection of open, normal, and short-circuit conditions without the need for further calibration, and current sensing multiplexing is allowed between channels to conserve analog-to-digital converter (ADC) resources. Each channel also implements adjustable current limits with an external resistor. Fig. 1 shows the typical application.

The device integrates short-circuit, over-current, thermal shutdown, short-to-battery and reverse current protections. Each channel has internal inductive clamp protection on the output during inductive switch-off. It can operate at ambient temperatures ranging from -40 °C to 125 °C and junction temperatures ranging from -40 °C to 150 °C with an HTSSOP16 package.

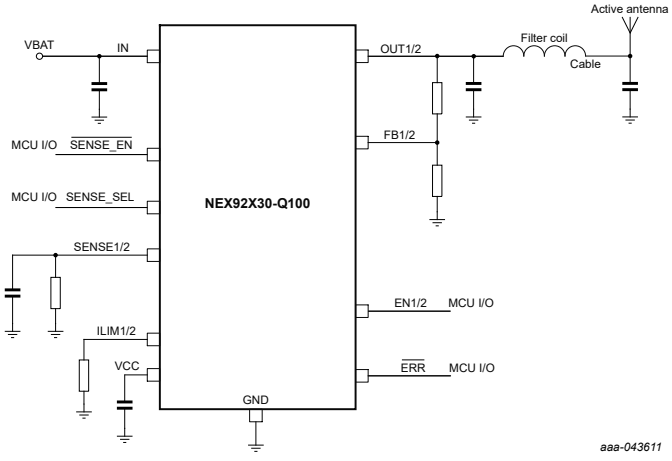


Fig. 1. Typical application

2. Features and benefits

- AEC-Q100 qualified for automotive applications
  - Ambient temperature (T_{amb}): -40 °C to 125 °C
  - Junction temperature (T_j): -40 °C to 150 °C
- Input voltage range: 4 V to 40 V (45 V transient)
- Output voltage range: 1.5 V to 20 V adjustable
- Maximum output current: 300 mA per channel
- High accuracy current sensing to detect antenna/MIC open conditions at low current
- Adjustable current limit by an external resistor
- High power supply ripple rejection (PSRR): typical 80 dB at 100 Hz
- Low dropout voltage:
  - 500 mV typical at 300 mA (V_{OUT} = 8.5 V)
- Stable with a wide range of ceramic output-stability cap:
  - ESR from 0.001 Ω to 5 Ω; output cap of 2.2 µF to 220 µF
- Integrated various fault protections:
  - Thermal shutdown
  - Short-circuit and over-current protection
  - Reverse-current protection
  - Output short-to-battery protection
  - Output inductive load clamp
  - Multiplexing current sensing between channels and devices
  - Ability to identify all faults with current sensing
  - 16-pin HTSSOP enhanced thermal pad package

3. Applications

- Infotainment active-antenna power supplies
- Automotive MIC power supplies
- Camera power supplies
- High-side power switches for small current applications

Table 1. Device information

Part number	Channel	Version
NEX92730DPCD-Q100	Dual	Latch
NEX92830DPCD-Q100	Dual	Auto-retry

4. Ordering information

Table 2. Ordering information

Type number	Temperature range (T_j)	Name	Description	Version
NEX92730DPCD-Q100	-40 °C to 150 °C	HTSSOP16	plastic, thermal enhanced thin shrink small outline package; 16 leads; 0.65 mm pitch; 5.0 mm x 4.4 mm x 1.2 mm body	SOT8108-1
NEX92830DPCD-Q100				

5. Marking

Table 3. Marking code

Type number	Marking code
NEX92730DPCD-Q100	N92730D
NEX92830DPCD-Q100	N92830D

6. Pin configuration and description

6.1. Pin configuration

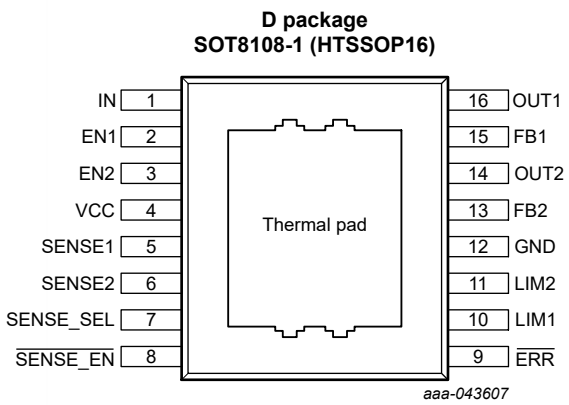


Fig. 2. Pin configuration

6.2. Pin description

Symbol	Pin	I/O	Description
IN	1	PWR	The input power-supply voltage pin should take the recommended value or a larger ceramic capacitor from IN to ground for optimal transient response and minimal input impedance. Place the input capacitor as close to the device's input as possible.
EN1	2	I	The enable logic pin activates the device when at a high level and disables it at a low level.
EN2	3	I	The enable logic pin activates the device when at a high level and disables it at a low level.
VCC	4	O	Internal 4.5 V regulator. Connect a 1 µF ceramic capacitor between VCC and GND for frequency compensation.
SENSE1	5	O	Output of current sensing for channel 1 sensing when SENSE_SEL and $\overline{\text{SENSE\_EN}}$ are low. To set the SENSE1 output voltage level, connect a resistor between this pin and GND. In addition, connect a 1 µF capacitor from this pin to GND for frequency compensation of the current-sense loop. Short this pin to GND if not used.
SENSE2	6	O	Output of current sensing for channel 2 sensing when SENSE_SEL and $\overline{\text{SENSE\_EN}}$ are low. To set the SENSE1 output voltage level, connect a resistor between this pin and GND. In addition, connect a 1 µF capacitor from this pin to GND for frequency compensation of the current-sense loop. Short this pin to GND if not used.
SENSE_SEL	7	I	This pin selects the current sensing between channel 1 and channel 2.
$\overline{\text{SENSE\_EN}}$	8	I	This pin enables and disables the current sensing pin for multiplexing, active-low enabled.
$\overline{\text{ERR}}$	9	O	Fault pin. It is an open-drain fault indicator for general faults.
LIM1	10	O	Programmable current-limit pin for channel 1. Connect a resistor to GND to set the current-limit level. This pin does not need an external capacitor. To set to internal current limit, short this pin to GND.
LIM2	11	O	Programmable current-limit pin for channel 2. Connect a resistor to GND to set the current-limit level. This pin does not need an external capacitor. To set to internal current limit, short this pin to GND.

Symbol	Pin	I/O	Description
GND	12	G	Ground pin. Connect this pin to the thermal pad with a low-impedance connection.
FB2	13	I	Feedback input for setting OUT2 voltage. Connect FB2 to GND for switch mode operation.
OUT2	14	PWR	Regulated output voltage pin for channel 2. A capacitor is required from OUT2 to ground for stability.
FB1	15	I	Feedback input for setting OUT1 voltage. Connect FB1 to GND for switch mode operation.
OUT1	16	PWR	Regulated output voltage pin for channel 1. A capacitor is required from OUT1 to ground for stability.
Thermal pad	Pad	-	The exposed thermal pad should be soldered to GND for improved thermal performance.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	input voltage	unregulated input	-42	45	V
V_{EN1}, V_{EN2}	enable voltage		-0.3	45	V
V_{OUT1}, V_{OUT2}	output voltage		-0.3	45	V
VCC	output voltage		-0.3	6.6	V
V_{SENSE1}, V_{SENSE2}	sense voltage		-0.3	VCC + 0.3	V
V_{LIM1}, V_{LIM2},	limit voltage		-0.3	6.6	V
$V_{\overline{SENSE\_EN}}$, V_{SENSE_SEL}, $V_{\overline{ERR}}$	sense control and fault voltage		-0.3	6.6	V
V_{FB1}, V_{FB2}	feedback voltage		-0.3	6.6	V
T_{amb}	ambient temperature		-40	125	°C
T_j	junction temperature		-40	150	°C
T_{stg}	storage temperature		-65	165	°C

[1] Stresses beyond those conditions under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8. ESD ratings

Table 5. ESD ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ESD}	electrostatic discharge voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 2 [1]	-2000	-	2000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C3 [2]	-1000	-	1000	V

[1] HBM stress testing was performed in accordance with AEC-Q100-002.
[2] CDM stress testing was performed in accordance with AEC-Q100-011.

9. Thermal information

Table 6. Thermal information

Thermal resistance according to JEDEC51-5 and -7.

Symbol	Parameter	SOT8108-1 (HTSSOP16)	Unit
$R_{\theta JA}$	junction to ambient thermal resistance	41.2	°C/W
$R_{\theta JC(top)}$	junction to case (top) thermal resistance	25.0	°C/W
$R_{\theta JB}$	junction to board thermal resistance	24.5	°C/W
Ψ_{JT}	junction to top char parameter	3.4	°C/W

10. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	input voltage		4		40	V
V_{EN1}, V_{EN2}	enable voltage		0		40	V
V_{OUT1}, V_{OUT2}	output voltage	normal-mode	1.5	-	20	V
		switch-mode	2	-	36	V
VCC	output voltage		0	-	5.3	V
V_{SENSE1}, V_{SENSE2}	sense voltage		0	-	5.3	V
V_{LIM1}, V_{LIM2},	limit voltage		0	-	5.3	V
$V_{\overline{SENSE\_EN}}$, V_{SENSE_SEL}, $V_{\overline{ERR}}$	sense control and fault voltage		0	-	5.3	V
V_{FB1}, V_{FB2}	feedback voltage		0	-	5.3	V
C_{OUT}	output capacitor stability range	[1]	2.2	-	220	µF
ESR	output capacitor ESR requirements	[2]	0.001	-	5	Ω
T_{amb}	ambient temperature		-40	-	125	°C
T_j	junction temperature		-40	-	150	°C

[1] Effective output capacitance of 1 µF minimum required for stability.

[2] Relevant ESR value at f = 10 kHz. If a large ESR capacitor is used, it is recommended to decouple it with a 100 nF ceramic capacitor to improve transient performance.

11. Electrical characteristics

Table 8. Electrical characteristics

At recommended operating conditions, T_j = -40 °C to 150 °C; C_{OUT} = 2.2 µF; V_{IN} = 13.5 V; I_{OUT} = 100 µA; V_{EN} = 2 V; unless otherwise noted, voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ[1]	Max	
Power supply						
V_{IN}	input voltage range		4	-	40	V
$V_{IN(UVLO)}$	under voltage lockout threshold	V_{IN} rising	3.4	3.6	3.8	V
		V_{IN} falling	3.0	3.2	3.4	V
		hysteresis	-	400	-	mV
V_{FB}	feedback voltage	voltage on FB pin	-1.5%	1.177	1.5%	V
I_q	quiescent current	V_{IN} = 5.5 V to 40 V; V_{OUT} = 5 V; I_{OUT1} = I_{OUT2} = 0 µA	-	340	550	µA
I_{GND}	operating current	V_{IN} = 13.5 V; V_{EN1} and V_{EN2} ≥ 1.3 V; V_{OUT1} = V_{OUT2} = 5 V; I_{OUT1} or I_{OUT2} = 300 mA	-	-	5.5	mA
I_{SHUT}	shutdown current	V_{EN1} = V_{EN2} = 0 V; V_{IN} = 4 V to 40 V	-	1	5	µA
Enable input (EN, EN1, EN2, $\overline{\text{SENSE\_EN}}$, and SENSE_SEL)						
V_{IL}	logic input low level	for EN, EN1, EN2, $\overline{\text{SENSE\_EN}}$, and SENSE_SEL	-	-	0.55	V
V_{IH}	logic input high level	for EN, EN1, EN2, $\overline{\text{SENSE\_EN}}$, and SENSE_SEL	1.4	-	-	V
I_{EN}	EN pin current	V_{EN} ≤ 40 V	-	-	5	µA
$I_{\overline{\text{SENSE\_EN}}}$	$\overline{\text{SENSE\_EN}}$ input current	$V_{\overline{\text{SENSE\_EN}}}$ = 5 V; V_{ENx} ≥ 1.3 V	-	-	1	µA
I_{SENSE_SEL}	SENSE_SEL input current	V_{SENSE_SEL} = 5 V; V_{ENx} ≥ 1.3 V	-	-	1.2	µA
Output						
V_{OUT}	output accuracy	V_{IN} = V_{OUT} + 1.5 V to 40 V (V_{IN} ≥ 4 V) I_{OUT} = 100 µA to 300 mA [2]	-1.5	-	1.5	%
$\Delta V_{OUT(\Delta VIN)}$	line regulation	V_{IN} = V_{OUT} + 1.5 V to 40 V (V_{IN} ≥ 4 V); I_{OUT} = 10 mA; voltage variation on FB pin	-	-	10	mV
$\Delta V_{OUT(\Delta IOUT)}$	load regulation	V_{IN} = V_{OUT} + 1.5 V to 40 V; (V_{IN} ≥ 4 V); I_{OUT} = 100 µA to 300 mA; voltage variation on FB pin	-	-	10	mV
V_{DO}	dropout voltage	V_{OUTx} = 8.5 V; I_{OUT} = 100 mA	-	165	320	mV
		V_{OUTx} = 8.5 V; I_{OUT} = 300 mA	-	500	950	mV
I_{OUT}	output current	V_{IN} = V_{OUT} + 1.5 V	-	-	300	mA
I_{CL}	output current limit	V_{IN} = V_{OUT} + 1.5 V; LIMx shorted to GND	340	-	550	mA
PSRR	power supply ripple rejection	V_{IN} = 13.5 V; V_{Ripple} = 0.5 V_{pp}; I_{OUT} = 10 mA; V_{OUT} = 5 V; C_{OUT} = 2.2 µF; frequency = 100 Hz [3]	-	80	-	dB

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ[1]	Max	
Current sensing and current limit						
I_{OUT}/I_{SENSE}	OUTx to SENSEx current ratio (I_{OUT}/I_{SENSE})	V_{IN} = 4 V to 40 V; I_{OUT} = 5 mA to 300 mA	-	198	-	-
	OUTx to SENSEx current ratio accuracy	I_{OUT} = 100 mA to 300 mA	-3	-	3	%
		I_{OUT} = 50 mA to 100 mA	-4	-	6	%
		I_{OUT} = 10 mA to 50 mA	-15	-	20	%
		I_{OUT} = 5 mA to 10 mA	-25	-	30	%
I_{OUT}/I_{LIM}	OUTx to LIMx current ration (I_{OUT}/I_{LIM})	V_{IN} = 4 V to 40 V; I_{OUT} = 50 mA to 300 mA	-	198	-	-
I_{LIMx}	programmable current-limit accuracy	V_{IN} = 4 V to 40 V; I_{OUT} = 50 mA to 300 mA	-8	-	8	%
I_{lkg}	SENSE, SENSE1, SENSE2, LIM, LIM1, and LIM2 leakage current	ENx = GND; T_{amb} = 25 °C	-	-	1	µA
V_{LIMx_th}	current-limit threshold voltage	voltage on the LIM; LIM1; and LIM2 pins when output current is limited	-	1.177	-	V
V_{SENSEx_stb}	current-sense short-to-battery fault voltage	voltage on SENSEx pin when short-to-battery or reverse current conditions are detected	3.05	3.2	3.3	V
V_{SENSEx_tsd}	current-sense thermal shutdown fault voltage	voltage on SENSEx pin when thermal shutdown is detected	2.7	2.85	3	V
V_{SENSEx_cl}	current-sense current-limit fault voltage	voltage on SENSEx pin when current-limit conditions are detected	2.4	2.55	2.65	V
I_{SENSEx_H}	current-sense fault condition current	current source current capacity when short-to-battery; reverse current; thermal shutdown; or current-limit conditions are detected [4]	3.3	-	-	mA
Fault detection						
V_{stb_th}	short-to-battery threshold	$V_{OUTx} - V_{IN}$; checked during turn-on sequence	-500	-55	110	mV
I_{REV}	reverse current detection level	power FET on (SW or LDO mode)	-120	-40	-1	mA
V_{R_th}	reverse protection voltage threshold	$V_{(OUTx)} - V_{IN}$ [4]	-	200	-	mV
V_{R_retry}	reverse protection auto-retry threshold	$V_{(OUTx)} - V_{IN}$ [4]	-	-300	-	mV
Interface circuitry						
$V_{\overline{ERR}\_L}$	$\overline{ERR}$ output low	I_{sink} = 5 mA	-	-	0.4	V
$I_{\overline{ERR}(lkg)}$	$\overline{ERR}$ open-drain leakage current	$\overline{ERR}$ high impedance; 5 V external voltage is applied at $\overline{ERR}$	-	-	1	µA
R_{OUTx_DIS}	OUT discharge resistor	ENx = GND [4]	-	50	-	kΩ
$I_{R(lkg)}$	reverse leakage current	-40 V < V_{IN} < 0 V; reverse current to IN	-	0.6	-	mA

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ[1]	Max	
VCC	internal voltage regulator	V_{IN} = 5.5 V to 40 V; I_{CC} = 0 mA	4.25	4.5	4.75	V
$I_{CC(LIM)}$	internal voltage regulator current limit		15	-	70	mA
Operating temperature range						
T_{SD}	junction thermal shutdown temperature	rising junction temperature	-	175	-	°C
T_{HYST}	thermal shutdown hysteresis		-	15	-	°C

[1] All typical values are measured at T_{amb} = 25 °C.
[2] External feedback resistor is not considered.
[3] Guaranteed by bench test, not fully tested in production.
[4] Guaranteed by bench test and design, not fully tested in production.

12. Switching characteristics

Table 9. Switching characteristics

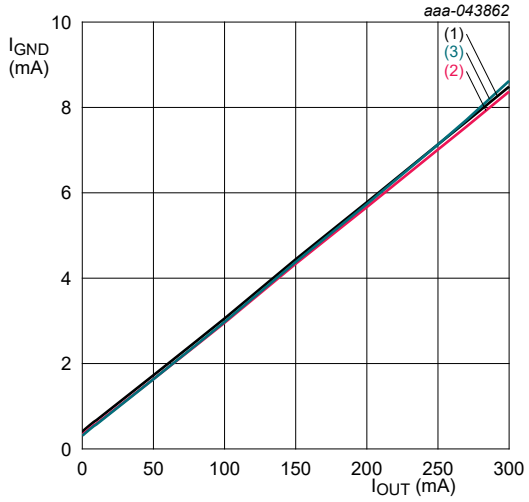
Symbol	Parameter	Conditions		T_{amb} = -40 °C to 125 °C			Unit
				Min	Typ	Max	
Current sensing and current limit							
$t_{d(SENSE\_SEL\_r)}$	current-sense delay time from the rising edge of SENSE_SEL	V_{ENx} ≥ 1.3 V; $\overline{SENSE\_EN}$ = GND; SENSE_SEL rise from 0 V to 5 V	[1]	-	10	-	µs
$t_{d(SENSE\_SEL\_f)}$	current-sense delay time from the falling edge of SENSE_SEL	V_{ENx} ≥ 1.3 V; $\overline{SENSE\_EN}$ = GND; SENSE_SEL fall from 5 V to 0 V	[1]	-	10	-	µs
$t_{d(\overline{SENSE\_EN}\_r)}$	current-sense delay time from rising edge of $\overline{SENSE\_EN}$	V_{ENx} ≥ 1.3 V; $\overline{SENSE\_EN}$ rise from 0 V to 5 V	[1]	-	10	-	µs
$t_{d(\overline{SENSE\_EN}\_f)}$	current-sense delay time from falling edge of $\overline{SENSE\_EN}$	V_{ENx} ≥ 1.3 V; $\overline{SENSE\_EN}$ fall from 5 V to 0 V	[1]	-	10	-	µs
Fault detection							
t_{PD_RC}	reverse current (short-to-battery) shutdown deglitch time	delay to shut down the switch or LDO after a drop over r_{on} becomes negative; I_{OUTx} = -200 mA (typical); T_{amb} = 25 °C		-	5	20	µs
t_{BLK_RC}	reverse current blanking time	V_{IN} = V_{OUT} + 1.5 V to 40 V; and V_{IN} ≥ 4 V I_{OUT} = 10 mA; voltage variation on FB pin		-	16	-	ms

[1] Design information, specified by design, not production tested.

13. Typical characteristics

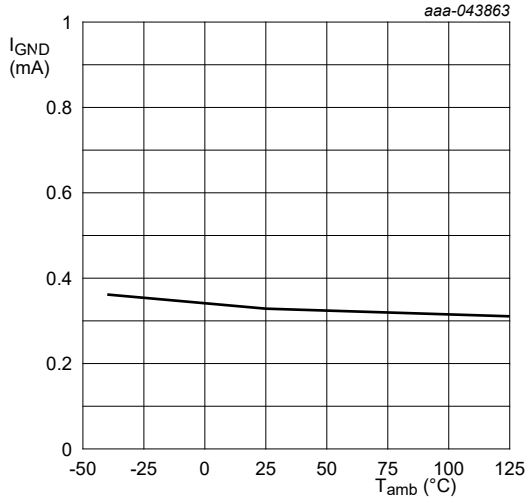
At recommended operating conditions, voltages are referenced to GND (ground = 0 V); typical values are at 25 °C (unless otherwise noted).

V_{IN} = 13.5 V; V_{EN} ≥ 1.3 V; C_{OUT} = 2.2 µF; V_{OUT} = 5 V; T_{amb} = -40 °C to 125 °C, unless otherwise specified.



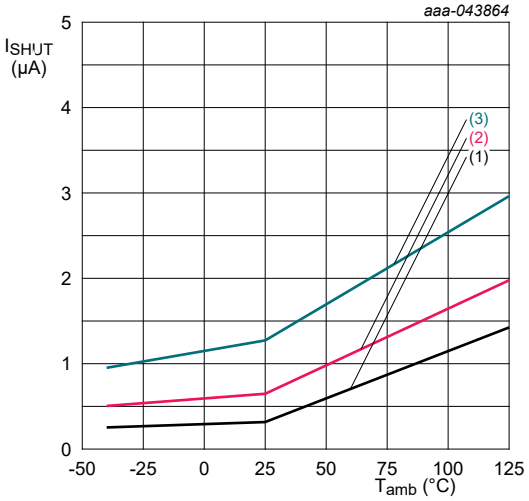
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 3. Ground current vs output current



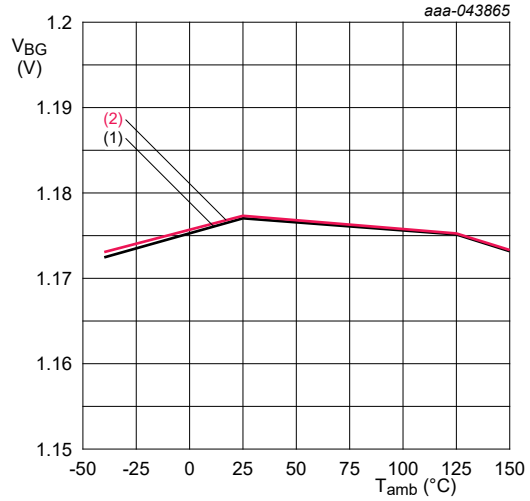
I_{OUT1} = I_{OUT2} = 0.2 mA

Fig. 4. Ground current vs ambient temperature



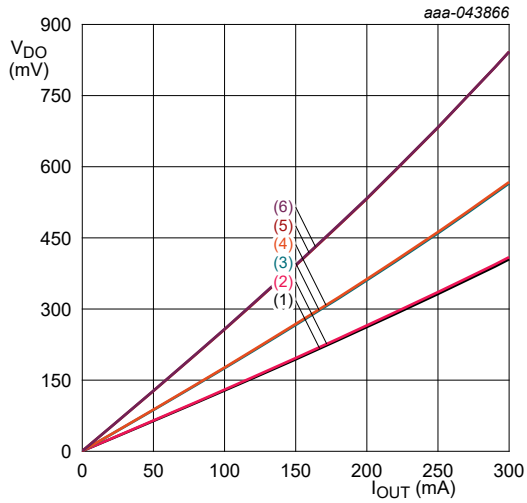
(1) V_{IN} = 4 V
(2) V_{IN} = 13.5 V
(3) V_{IN} = 40 V

Fig. 5. Shutdown current vs ambient temperature



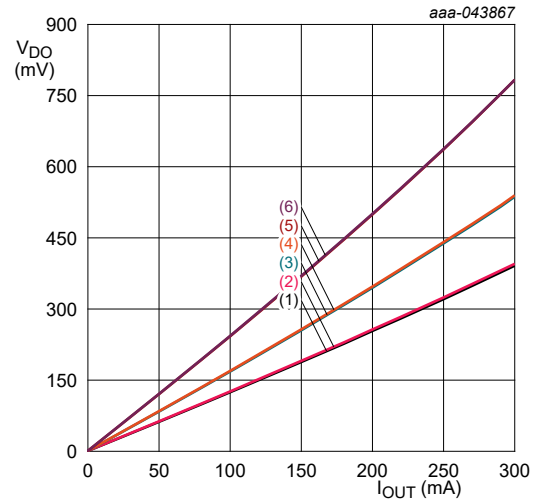
I_{OUT1} = I_{OUT2} = 10 mA
(1) Channel 1
(2) Channel 2

Fig. 6. Bandgap voltage (FB) vs ambient temperature



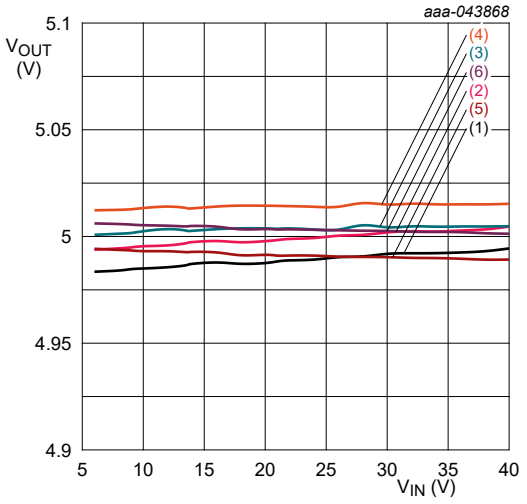
$V_{OUT1} = V_{OUT2} = 5$ V
(1) T_{amb} = -40 °C; channel 1
(2) T_{amb} = -40 °C; channel 2
(3) T_{amb} = 25 °C; channel 1
(4) T_{amb} = 25 °C; channel 2
(5) T_{amb} = 125 °C; channel 1
(6) T_{amb} = 125 °C; channel 2

Fig. 7. Dropout voltage vs output current



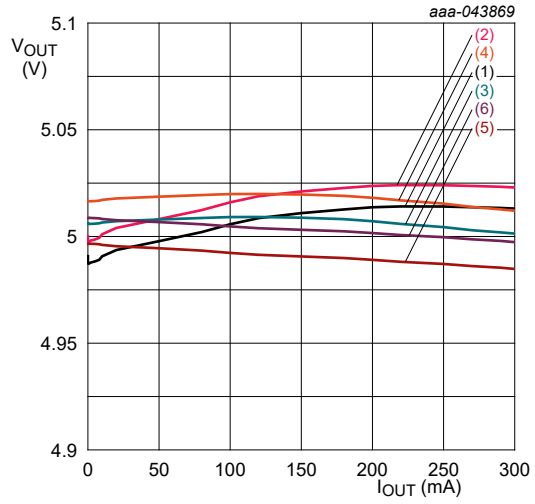
$V_{OUT1} = V_{OUT2} = 8.5$ V
(1) T_{amb} = -40 °C; channel 1
(2) T_{amb} = -40 °C; channel 2
(3) T_{amb} = 25 °C; channel 1
(4) T_{amb} = 25 °C; channel 2
(5) T_{amb} = 125 °C; channel 1
(6) T_{amb} = 125 °C; channel 2

Fig. 8. Dropout voltage vs output current



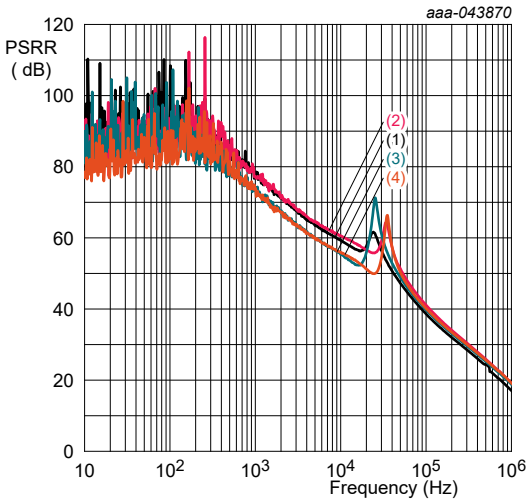
$V_{OUT} = 5$ V; $I_{OUT} = 10$ mA
(1) T_{amb} = -40 °C; V_{OUT1}
(2) T_{amb} = -40 °C; V_{OUT2}
(3) T_{amb} = 25 °C; V_{OUT1}
(4) T_{amb} = 25 °C; V_{OUT2}
(5) T_{amb} = 125 °C; V_{OUT1}
(6) T_{amb} = 125 °C; V_{OUT2}

Fig. 9. Line regulation vs input voltage



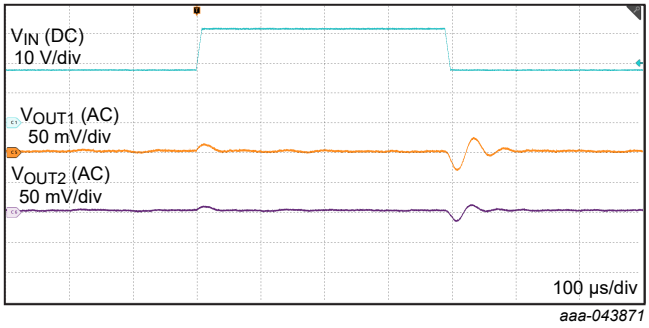
$V_{OUT} = 5$ V, $V_{IN} = 13.5$ V
(1) T_{amb} = -40 °C; V_{OUT1}
(2) T_{amb} = -40 °C; V_{OUT2}
(3) T_{amb} = 25 °C; V_{OUT1}
(4) T_{amb} = 25 °C; V_{OUT2}
(5) T_{amb} = 125 °C; V_{OUT1}
(6) T_{amb} = 125 °C; V_{OUT2}

Fig. 10. Load regulation vs output current



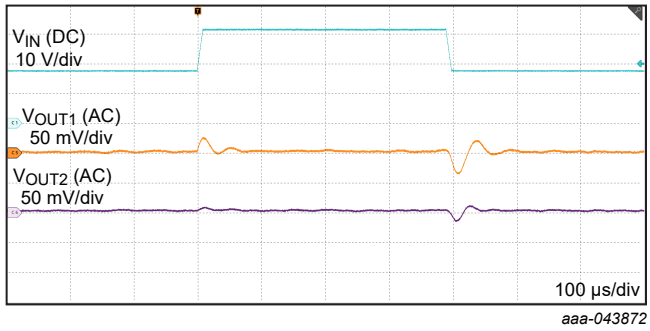
V_{IN} = 13.5 V; C_{OUT} = 10 µF
(1) V_{OUT2} = 5 V; I_{OUT} = 10 mA
(2) V_{OUT2} = 5 V; I_{OUT} = 100 mA
(3) V_{OUT1} = 8.5 V; I_{OUT} = 10 mA
(4) V_{OUT1} = 8.5 V; I_{OUT} = 100 mA

Fig. 11. PSRR vs frequency



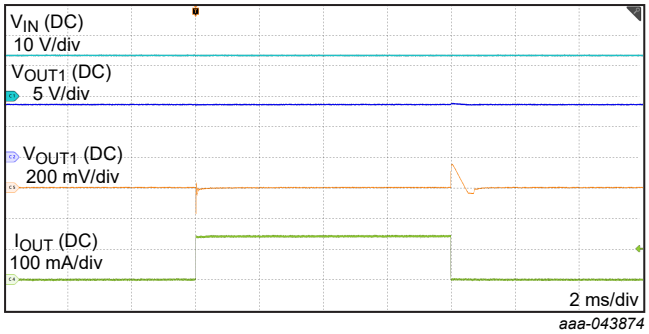
V_{IN} = 9 V to 16 V; slew rate = 1 V/µs;
V_{OUT1} = 8.5 V; V_{OUT2} = 5 V;
I_{OUT} = 50 mA; C_{OUT} = 10 µF

Fig. 12. Line transient



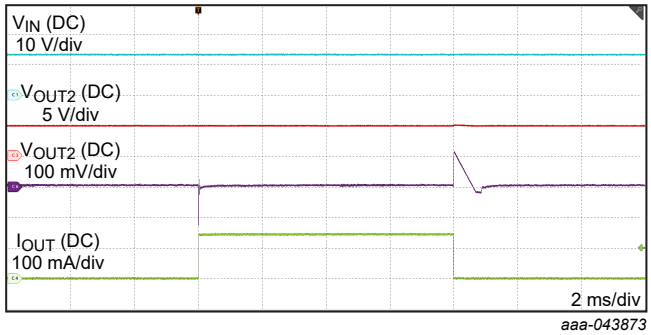
V_{IN} = 9 V to 16 V; slew rate = 1 V/µs;
V_{OUT1} = 8.5 V; V_{OUT2} = 5 V;
I_{OUT} = 100 mA; C_{OUT} = 10 µF

Fig. 13. Line transient



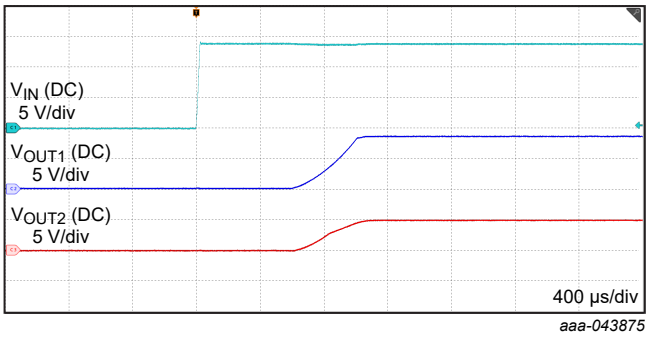
V_{IN} = 13.5 V; I_{OUT} = 0 mA to 150 mA;
slew rate = 1 A/µs; V_{OUT1} = 8.5 V; C_{OUT} = 10 µF

Fig. 14. Load transient



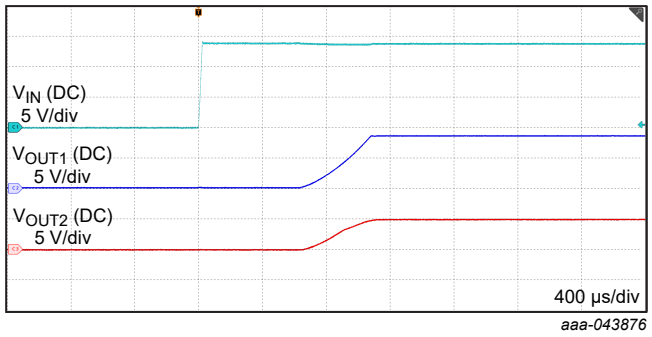
V_{IN} = 13.5 V; I_{OUT} = 0 mA to 150 mA;
slew rate = 1 A/µs; V_{OUT2} = 5 V; C_{OUT} = 10 µF

Fig. 15. Load transient



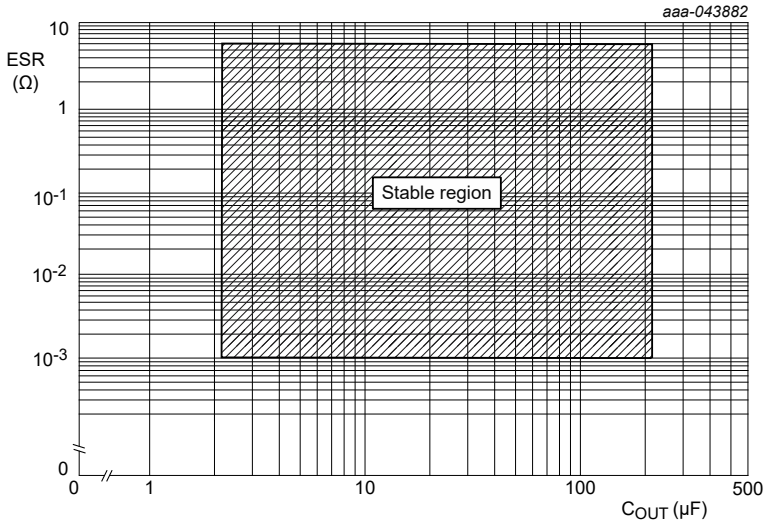
V_{OUT1} = 8.5 V; V_{OUT2} = 5 V; C_{OUT} = 10 µF;
I_{OUT} = 50 mA; V_{IN} from 0 V to 14 V

Fig. 16. Start up



V_{OUT1} = 8.5 V; V_{OUT2} = 5 V; C_{OUT} = 10 µF;
I_{OUT} = 100 mA; V_{IN} from 0 to 14 V

Fig. 17. Start up



ESR from 0.001 Ω to 5 Ω; output cap of 2.2 µF to 220 µF

Fig. 18. Stability, ESR vs C_{OUT}

14. Detailed description

14.1. Overview

The NEX92x30-Q100 devices feature a dual-channel, high-voltage LDO with the current sensing function. The devices operate with a wide input voltage range of 4 V to 40 V (45 V load dump protection). They also offer protection of antenna lines against electrostatic discharge (ESD) and prevention from short-to-ground, short-to-battery, and thermal over-stress. Device output voltage is adjustable from 1.5 V to 20 V through an external resistor divider.

Alternatively, each channel can be configured as a switch. These devices monitor the load current. Accurate current sensing allows for detection of open, normal, and short to ground conditions without the need of further calibration. Current sensing can also be multiplexed between channels and devices to save ADC resources. Each channel also provides an adjustable current limit with an external resistor.

14.2. Functional block diagram

The NEX92x30-Q100 block diagram as below Fig. 19 shown.

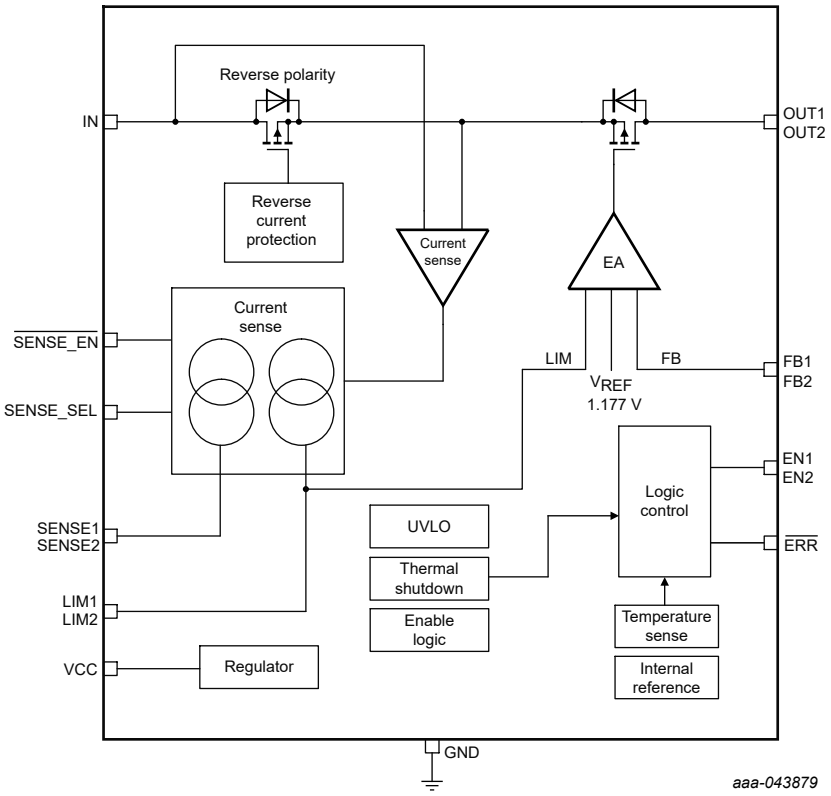


Fig. 19. Functional block diagram

14.3. Feature description

14.3.1. Fault detection and protection

The device includes both analog current sensing and digital fault pins for full diagnostics of different fault conditions. The current sensing voltage scale is selected based on the output current range of requirements. Fig. 20 shows a recommended setting that allows for full diagnostics of each fault.

Before the device goes into current-limit mode, the output current sensing voltage is linearly proportional to the actual load current. During a thermal shutdown and short-to-battery condition, the current sensing voltage is set to the fault voltage level that is specified in Table 8.

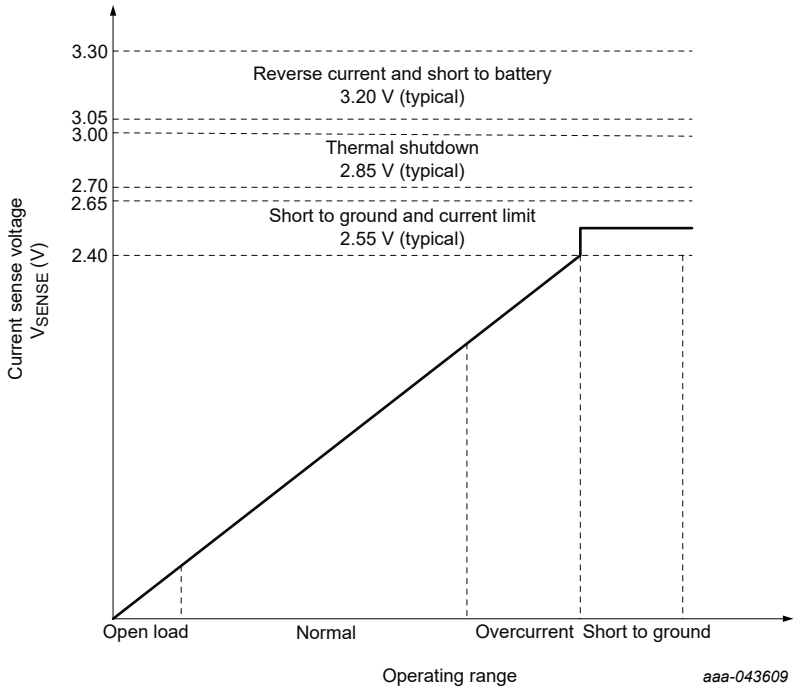


Fig. 20. Functionality of the current-sense output

14.3.2. Short-circuit and current-limit protection

The current limit on each channel is programmed by selecting the external resistor. The voltage on LIMx pin is compared with an internal voltage reference. When the threshold is exceeded, the current limit is triggered. The output of the current-limited channel continues to remain on, and the current is limited.

Under current-limit status, the $\overline{ERR}$ pin asserts low, and the SENSE voltage of the fault channel is internally pulled up to a voltage rail between 2.4 V and 2.65 V as shown in Fig. 20. At this moment, the output voltage is not disabled. The Microcontroller Unit (MCU) should monitor the voltage at the SENSEx pin or $\overline{ERR}$ pin ($\overline{ERR}$ pin does not only indicate current-limit fault, refer to Table 10) to disable the faulted channel by pulling the ENx pin low. If a current-limit condition exists for a long period, thermal shutdown can be triggered and the output is shut down.

14.3.3. Short-to-battery and reverse current detection

Shorting the OUT pin to the battery due to a fault in the vehicle system is possible. Each channel detects this failure by comparing the voltage at the OUT and IN pins before the switch turns on. Each time the LDO switch is enabled on the rising edge of the EN pin or during the exiting of the thermal shutdown, the short-to-battery detection occurs. At this moment, if the device detects the short-to-battery fault, the LDO switch is latched off, the $\overline{ERR}$ pin is asserted low, and the fault-channel SENSE voltage is pulled up internally to a voltage rail between 3.05 V and 3.3 V.

During normal operation, if a short-to-battery fault results in reverse current for 5 µs (typical), the device is latched off and $\overline{ERR}$ pin is asserted low. The device works normally when the short-to-battery is removed and the EN pin must be toggled. Or with the auto-retry version, the device keeps monitoring the input and output voltage. Once input voltage is higher than the output voltage, the device resumes normal operation. It is not necessary to toggle the EN pin.

Series inductance and the output capacitor can produce ringing during power-up or recovery from current-limit, resulting in an output voltage that temporarily exceeds the input voltage. The 16 ms (typical) reverse-current blanking can help filter this ringing.

For the dual-channel antenna LDO application, if both channels are enabled and one channel is shorted to ground after power-up, the current drawn from the input capacitor can result in a temporary dip in the input voltage, which can trigger the reverse-current detection fault. To prevent this false trigger event, care must be taken when selecting the input capacitor. An increase of the input capacitor value is recommended.

14.3.4. Current-limit operation

The device features an internal current-limit circuit that protects the regulator during transient high-load current faults or shorting events.

When the device is in current limit mode, the output voltage is not regulated. During a current-limit event, the device heats up due to increased power dissipation. When the device reaches the current limit (I_{CL}), the pass transistor dissipates power according to the formula [(V_{IN} – V_{OUT}) x I_{CL}].

If thermal shutdown is triggered, the device will turn off. Once it cools down, the internal thermal shutdown circuit will turn the device back on. If the output current fault condition persists, the device will cycle between current-limit and thermal shutdown.

14.3.5. Thermal shutdown

The NEX92x30-Q100 integrates an internal temperature sensor to monitor the junction temperature (T_j). If T_j exceeds the thermal shutdown temperature (T_{SD}) of 175 °C, the device ceases operation. The device will resume functioning when T_j drops below the hysteresis threshold of approximately 15 °C.

Thermal shutdown may be triggered during start-up due to large inrush currents charging substantial output capacitance, or under heavy loads where high (V_{IN} – V_{OUT}) regulations result in significant power dissipation across the die. Proper heat sinking should be considered in these high power dissipation scenarios.

Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability and device lifetime. The SENSE voltage is internally pulled up to a voltage rail between 2.7 V and 3 V during T_{SD} status.

14.3.6. Integrated reverse-polarity protection

The device integrates a reverse-connected PMOS to block the reverse current during reverse polarity at the input and output short-to-battery condition. A special ESD structure at the input is specified to withstand -42 V. Table 10 shows the fault table to indicate which failure occurs.

Table 10. Fault fable

Failure mode	V_{SENSE}	$\overline{ERR}$	LDO switch output	Latched	
				NEX92730D-Q100	NEX92830D-Q100
Open load	I_{OUT} x $R_{(SENSE)}$/198	High	Enable	No	No
Normal		High	Enable	No	No
Over-current		High	Enable	No	No
Short-circuit or current-limit	2.4 V to 2.65 V	Low	Enable	No	No
Thermal shutdown	2.7 V to 3 V	Low	Disable	No	No
Output short-to battery	3.05 V to 3.3 V	Low	Disable	Yes	No (auto-retry)
Reverse current	3.05 V to 3.3 V	Low	Disable	Yes	No (auto-retry)

14.3.7. Integrated inductive clamp

During output turnoff, the cable inductance continues to source the current from the output of the device. The device integrates an inductive clamp to help dissipate the inductive energy stored in the cable. An internal diode is connected between OUT and GND pins with a DC-current capability of 300 mA for inductive clamp protection.

14.3.8. Undervoltage lockout (UVLO)

The device includes an undervoltage lockout (UVLO) threshold that is internally fixed. The undervoltage lockout activates when the input voltage on the IN pin drops below $V_{IN(UVLO)}$. The UVLO makes sure that the regulator is not latched into an unknown state during low input supply voltage.

If the input voltage has a negative transient that drops below the UVLO threshold and then recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above the required levels.

14.3.9. Enable (EN1 and EN2)

The NEX92x30-Q100 devices feature two active-high enable inputs, EN1 and EN2. The EN1 pin controls output voltage 1 (OUT1), and the EN2 pin controls output voltage 2 (OUT2).

The devices consume a maximum of shutdown current at 5 µA when the ENx pins are low. Both the EN1 and EN2 pins have a maximum internal pulldown of 5 µA.

In addition, the enable logic can support 3.3 V and 1.8 V IO level, and it is well compatible with 5 V/3.3 V and 1.8 V MCU/SoC.

14.3.10. Internal voltage regulator (VCC)

The devices feature an internal regulator that regulates the input voltage to 4.5 V to power all internal circuitry. It bypasses a 1 µF ceramic capacitor from the VCC pin to the GND pin for frequency compensation. The VCC pin can be used as a power supply for external circuitry with up to 15 mA current capability.

14.3.11. Current sensing multiplexing

The two independent current sensing pins (one for each channel) provide flexibility in the system design. When the ADC resource is limited, the device allows the multiplexing of the current sensing pins by only using one current sensing pin and one ADC to monitor all the antenna outputs.

The SENSE_SEL pin selects the channels to monitor the current. The $\overline{\text{SENSE\_EN}}$ pin enables and disables the SENSE pin, allowing multiplexing between chips. Therefore, only one ADC and one resistor is needed for current sensing diagnostics of multiple outputs. When the SENSE1 pin is connected to an ADC, the current flows through both channels can be sensed by changing the electrical level at the SENSE_SEL pin.

Table 11 lists the selection logic for the current sensing.

Table 11. $\overline{\text{SENSE\_EN}}$ and SEN_SEL logic table

$\overline{\text{SENSE\_EN}}$	SENSE_SEL	SENSE 1 status	SENSE 2 status
Low	Low	CH1 current	CH2 current
Low	High	CH2 current	High impedance
High	-	High impedance	High impedance

Fig. 21 shows the application of four antenna channels sharing one ADC resource.

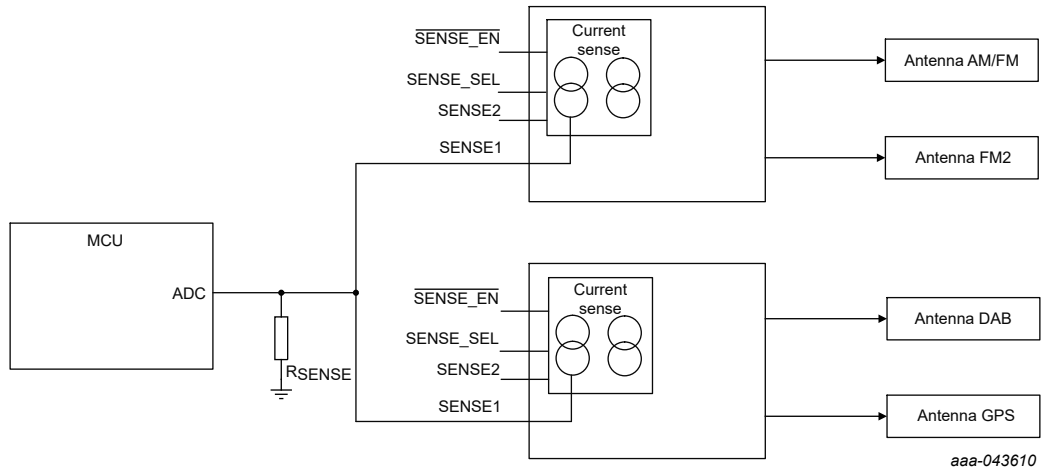


Fig. 21. Current multiplexing application block

14.3.12. Adjustable output voltage (FB1 and FB2)

Use an external resistor divider and select an output voltage between 1.5 V and 20 V. The recommended value for both R1 and R2 is less than 100 kΩ.

$$V_{OUT} = \frac{V_{FB} \times (R1 + R2)}{R2} \quad (1)$$

Where V_{FB} = 1.177 V (typical).

The devices can also be configured as a current-limited switch by connecting the FBx pin to the GND pin.

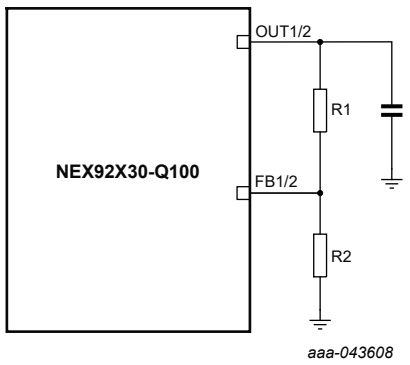


Fig. 22. Output voltage setting connection

15. Application implementation

15.1. Application information

The following section is a reference to simplify the system design with the NEX92x30-Q100 typical application for external components calculation and selection.

15.2. Typical application

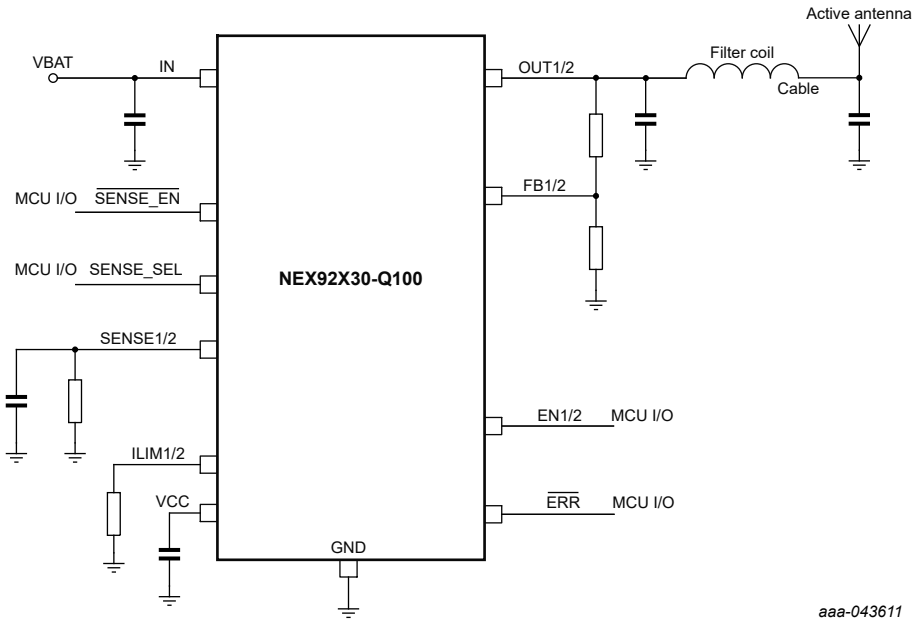


Fig. 23. NEX92x30-Q100 typical application

15.2.1. Design requirements

A typical application is applied in automotive and power supply for AM/FM antenna, which normally requires 8.5 V or 5 V output. The design parameters are listed in Table 12.

Table 12. Design parameters

Parameters	Values
Input voltage	4 V to 40 V
Output voltage	1.5 V to 20 V
Output capacitor range	2.2 µF to 220 µF
Output capacitor ESR range	0.001 Ω to 5 Ω
SENSE resistor	Refer to Section 15.2.2.3
Programmable current limit	50 mA to 300 mA
Auto-retry required	Yes

15.2.2. Detailed design procedure

15.2.2.1. Input capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 2.2 µF. The voltage rating must be greater than the maximum input voltage.

15.2.2.2. Output capacitor

To ensure the stability of the NEX92x30-Q100, the device requires an output capacitor with a value of 2.2 µF to 220 µF from OUT to GND and ESR range between 0.001 Ω and 5 Ω. It is recommended to select a ceramic capacitor with low ESR to improve the load transient response and ripple performance.

15.2.2.3. Current sensing resistor selection

The current-sense outputs, SENSEx (SENSE1 and SENSE2), are proportional to the output current at the OUT1 and OUT2 pins with a factor of 1/198. An output resistor, R_{SENSEx}, must be connected between the SENSEx pin and ground to generate a current sensing voltage to be sampled by ADC. Use equation (2) to calculate the voltage at SENSEx pin (V_{SENSEx}).

$$V_{SENSEx} = I_{SENSEx} \times R_{SENSEx} \quad (2)$$

Where $I_{SENSEx} = \frac{I_{OUTx}}{198}$.

For this example, 1.5 kΩ selected as a value for R_{SENSEx}. Ignore the resistor and current sensing accuracy. If the load current equals to 198 mA, use equation (3) to get V_{SENSEx} voltage.

$$I_{SENSEx} = \frac{I_{OUTx}}{198} = 1 \quad mA \quad (3)$$

Then V_{SENSEx} can be calculated as 1 mA x 1.5 kΩ = 1.5 V.

To prevent any overlap between normal operation and current-limit or short-to-ground phase, it is recommended to use equation (4) to select the value of the SENSE resistor.

$$R_{SENSEx} \leq \frac{198 \times 2.4\ V}{I_{OUT(max)}} \quad (4)$$

Where:

- 198 is the output current to current-sense ratio.
- 2.4 V is the minimum possible voltage at the SENSEx pin under a short-circuit fault case.
- $I_{OUT(max)}$ is the maximum possible output current under normal operation.

To stabilize the current-sense loop, connecting a 1 µF ceramic capacitor at the SENSE1, or SENSE2 pin is required. Table 13 lists the current sensing accuracy across temperature.

Table 13. Current sensing accuracy

Output current	Current sensing accuracy
10 mA to 50 mA	20%
50 mA to 100 mA	6%
100 mA to 300 mA	3%

15.2.2.4. Current-limit resistor selection

The current at the LIMx pins (LIM1 and LIM2) is proportional to the load current at the OUTx (OUT1 and OUT2) pins and is internally connected to a current-limit comparator referenced to 1.177 V.

The current limit is programmable through the external resistor connected at LIMx pin. Use equation (5) to calculate the value of the external resistor, R_{LIMx}. The programmable current-limit accuracy is 8% maximum across all conditions. The internal current limit of the device is set by shorting the LIM pin to ground.

Since the current limit varies by 8%, equations (7) and (8) show how to calculate the minimum and maximum current-limit value.

$$R_{LIMx} = \frac{1.177\ V}{I_{LIMx}} \times 198 \quad (5)$$

Where:

$$I_{LIMx(typ)} = \frac{1.177\ V}{R_{LIMx}} \times 198 \quad (6)$$

$$I_{LIMx(min)} = I_{LIMx(typ)} \times (1 - 8\%) \quad (7)$$

$$I_{LIMx(max)} = I_{LIMx(typ)} \times (1 + 8\%) \quad (8)$$

Note that this result does not include resistor tolerance in the calculation. To make sure that the current does not exceed the set amount, resistor tolerance must also be included in the equation.

15.2.2.5. Auto-retry and latch behavior

The NEX92x30-Q100 devices include latch and auto-retry versions to provide tailored solutions based on application requirements.

- Auto-retry version (NEX92830-Q100): automatically resumes operation when $V_{IN} > V_{OUT}$ + 300 mV (typical)
- Latch version (NEX92730-Q100): requires toggling EN or V_{IN} to restart

The following examples illustrate the behavioral differences in practical applications: short-to-battery and reverse current.

Case 1: Short-to-batty event, the device starts with output shorted to battery, battery is subsequently removed

- Auto-retry behavior: The output recovers automatically without toggling V_{IN} or EN. When enabled after an initial output short-to-battery condition, the device recovers normally after battery removal. SENSEx and $\overline{ERR}$ signals return to normal indication. Refer to Fig. 24 for more information.
- Latch behavior: The device disables the output upon detecting a short-to-battery fault and remains latched off. SENSEx and $\overline{ERR}$ retain fault indications until EN or V_{IN} is toggled. Refer to Fig. 25 for more information.

Case 2: Reverse current event, V_{IN} or EN is rapidly cycled while output capacitance remains charged

- Auto-retry behavior: Output recovers normally even when voltage does not fully discharge between cycles. SENSEx and $\overline{ERR}$ signals return to normal indication. Refer to Fig. 26 for more information.
- Latch behavior: The device detects reverse current, disables the output, and latches off. SENSEx and $\overline{ERR}$ maintain fault indications until EN or V_{IN} is toggled. Refer to Fig. 27 for more information.

Table 14. Waveforms of case 1 and 2

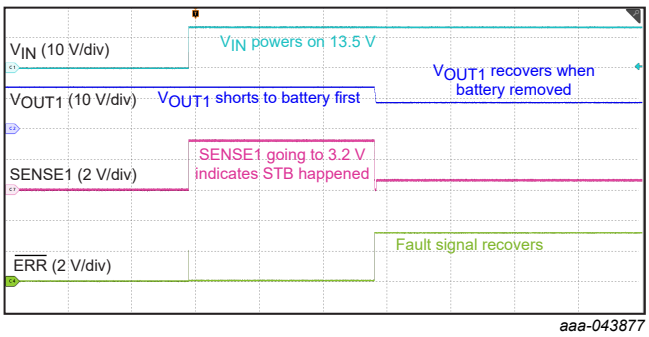


Fig. 24. Case 1: output short-to-battery (auto-retry)

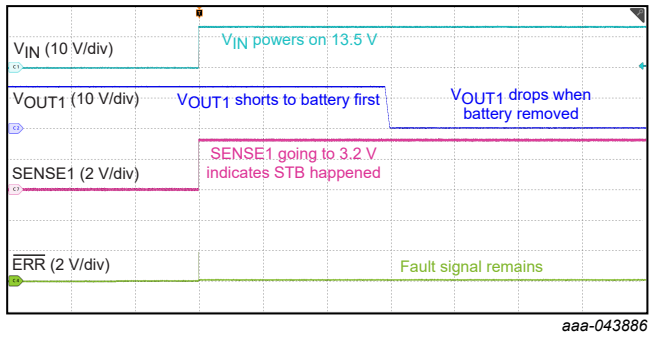


Fig. 25. Case 1: output short-to-battery (latch)

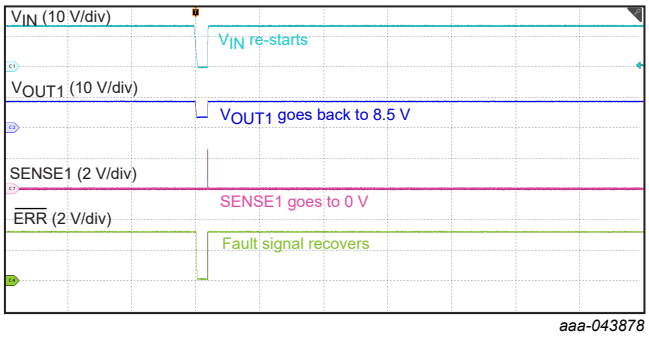


Fig. 26. Case 2: big output capacitor (auto-retry)

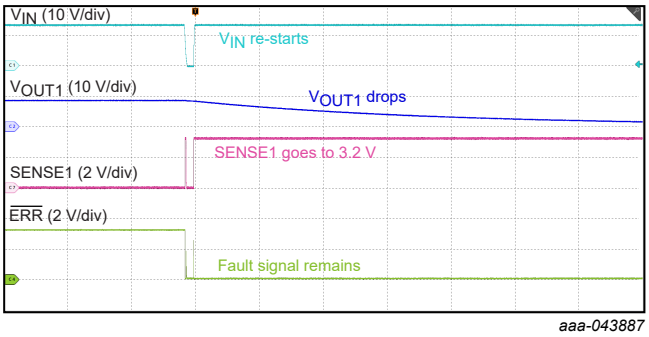


Fig. 27. Case 2: big output capacitor (latch)

16. Layout

16.1. Layout guidelines

For optimal overall performance, the following guidelines are recommended for an LDO layout:

- Place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections.
- Ensure ground return connections for the input and output capacitors, as well as the LDO ground pin, are as close to each other as possible, connected by a wide copper surface on the component side.
- Avoid using vias and long traces to connect the input and output capacitors, as this can negatively impact system performance.
- In most applications, a ground plane is essential to meet thermal requirements.

A ground reference plane should be either embedded in the PCB or located on the bottom side opposite the components. This reference plane helps ensure output voltage accuracy, shields against noise, and acts as a thermal plane to dissipate heat from the LDO device when connected to the thermal pad.

16.2. Layout examples

Fig. 28 shows the layout example of NEX92x30-Q100 (HTSSOP16) dual-channel devices.

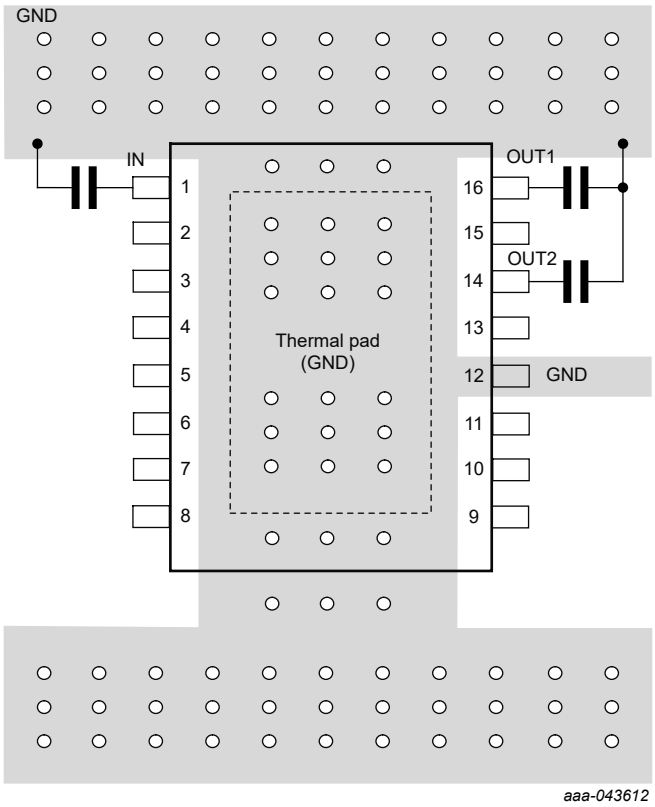
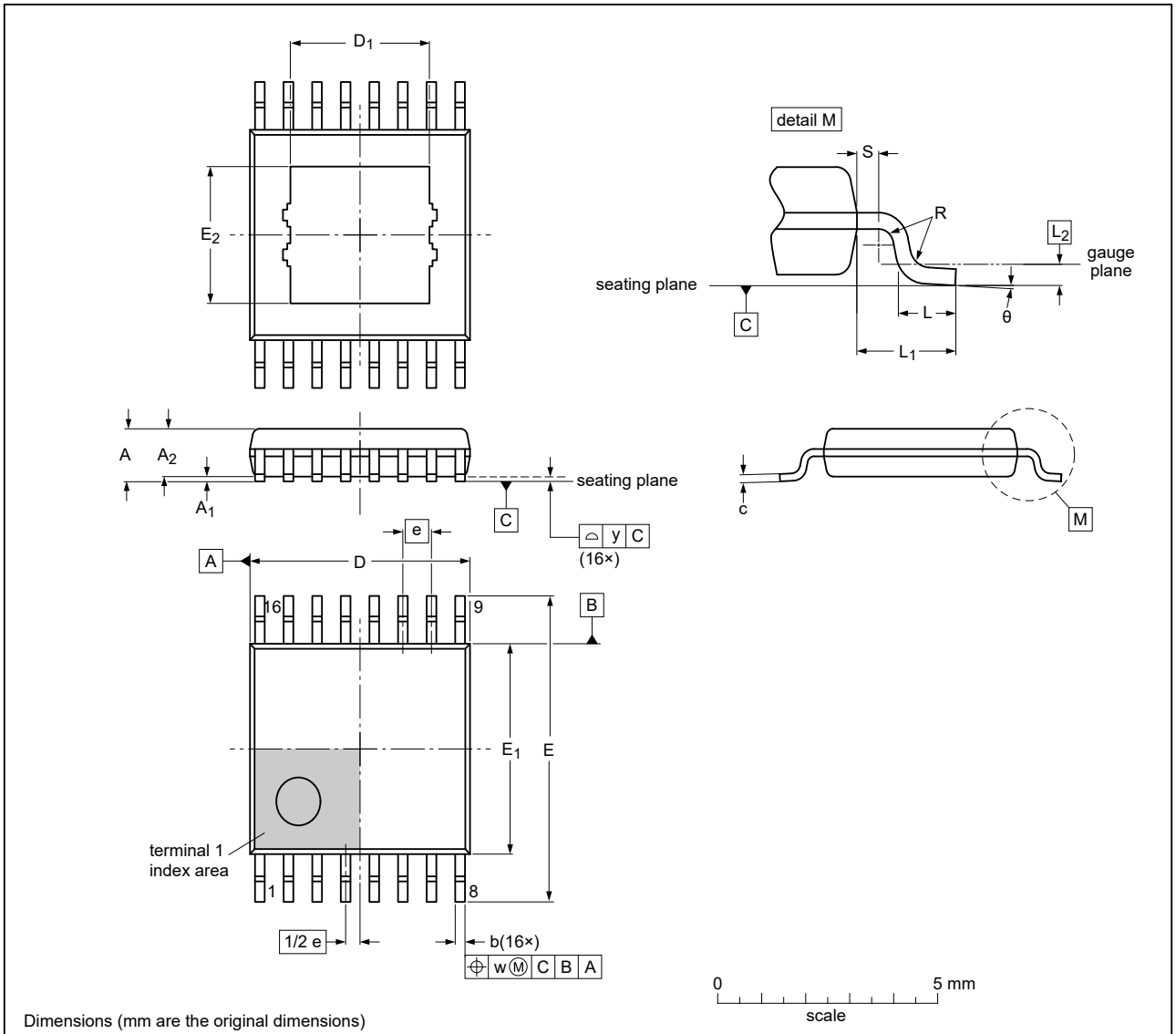


Fig. 28. NEX92x30-Q100 dual-channel layout example

17. Package outline

plastic, thermal enhanced thin shrink small outline package;
16 leads, 0.65mm pitch, 5.0mm × 4.4mm × 1.2mm body **SOT8108-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	b	c	D	D_1	E	E_1	E_2	e	L	L_1	L_2	R	S	y	w	θ
mm	max	1.20	0.15	1.05	0.29	0.20	5.10	3.16	6.60	4.50	2.86	0.65	0.75	1.00	0.25					8°
	nom			1.00			5.00	REF	6.40	4.40	REF	BSC	0.60	REF	BSC			0.10	0.10	
	min		0.05	0.80	0.20	0.15	4.90		6.20	4.30			0.45			0.09	0.20			0°

Note
1. Dimension D does not include mold flash, protrusion or gate burrs.
Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end or per side.
2. Dimension E_1 does not include interlead flash or protrusion that shall not exceed 0.25 mm per side.

sot8108-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8108-1						25-07-17

Fig. 29. Package outline SOT8108-1 (HTSSOP16)

18. Abbreviations

Table 15. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AM	Amplitude Modulation
ANSI	American National Standards Institute
BCM	Body Control Module
CDM	Charge Device Model
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
EV	Electric Vehicle
FM	Frequency Modulation
HBM	Human Body Model
HEV	Hybrid Electric Vehicle
JEDEC	Joint Electron Device Engineering Council
LDO	Low-Dropout
MCU	Microcontroller Unit
MIC	Mechanical Instrument Cluster
PSRR	Power Supply Ripple Rejection
SoC	System-on-a-Chip
UVLO	Undervoltage Lockout

19. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX92x30_Q100 v. 1	20250801	Product data sheet	-	-

20. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

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